What Is Claimed Is:

1. A liquid crystal display device, comprising:

first and second substrates having an active region, data and gate pad portions, and gate and data link portions;

a sealant pattern within a sealant region;

at least one first dummy pattern provided between adjacent ones of the gate link portions;

at least one second dummy pattern provided between adjacent ones of the data link portions; and

a liquid crystal layer between the first and second substrates,

wherein a width of each of the first and second dummy patterns is less than a width of the sealant pattern.

2. The device according to claim 1, wherein the width of the first and second dummy patterns are each less than about 3/4 of the width of the sealant pattern.

3. The device according to claim 1, wherein each of the gate link portions comprise:

a gate metal layer on the first substrate;

a gate insulating layer on the gate metal layer;

a semiconductor layer on the gate insulating layer; and

a passivation layer on the semiconductor layer.

4. The device according to claim 1, wherein each of the data link portions comprise:

a gate insulating layer on the first substrate;

a semiconductor layer on the gate insulating layer;

a data metal layer on the gate insulating layer; and

a passivation layer on the data metal layer.

5. The device according to claim 1, wherein the first dummy pattern comprises:

a gate metal layer on the first substrate;

a gate insulating layer on the gate metal layer;

a semiconductor layer on the gate insulating layer; and

a passivation layer on the gate insulating layer.

6. The device according to claim 1, wherein the second dummy pattern comprises:

a gate insulating layer on the first substrate;

a semiconductor layer on the gate insulating layer;

a data metal layer on the gate insulating layer; and

a passivation layer on the data metal layer.

7. The device according to claim 1, wherein a height of the gate link portions and a height of the data link portions are substantially the same.

8. A liquid crystal display device, comprising:

first and second substrates having an active region, data and gate link portions, and a sealant region;

at least one first dummy pattern on the first substrate disposed between adjacent ones of the data link portions;

at least one second dummy pattern on the first substrate disposed between adjacent ones of the gate link portions;

a sealant pattern within the sealant region completely covering the dummy pattern; and

a liquid crystal layer between the first and second substrates,

wherein the first dummy pattern is substantially identical to the data link portions, and the second dummy pattern is substantially identical to the gate link portions.

9. The device according to claim 8, wherein the gate link portions and the data link portions have substantially identical layers.

10. The device according to claim 8, wherein the first dummy pattern comprises:

a gate metal layer on the first substrate;

a gate insulating layer on the gate metal layer;

a semiconductor layer on the gate insulating layer; and

a passivation layer on the gate insulating layer.

11. The device according to claim 8, wherein the second dummy pattern includes:

a gate insulating layer on the first substrate;

a semiconductor layer on the gate insulating layer;

a data metal layer on the gate insulating layer; and

a passivation layer on the data metal layer.

12. A method of fabricating a liquid crystal display device, comprising:

providing first and second substrates having an active region, gate and data link portions, and a sealant region;

forming a first dummy pattern within the sealant region between adjacent ones of the gate link portions;

forming a second dummy pattern within the sealant region between adjacent ones of the data link portions;

forming a sealant pattern within the sealant region to cover the first and second dummy patterns; and

attaching the first and second substrates.

13. The method according to claim 12, wherein forming the first dummy pattern includes:

forming a gate metal layer on the first substrate;

forming a gate insulating layer and a semiconductor layer on the gate metal layer; and

forming a passivation layer on the semiconductor layer.

14. The method according to claim 12, wherein forming the second dummy pattern includes:

forming a gate insulating layer and a semiconductor layer on the first substrate;

forming a data metal layer on the semiconductor layer; and

forming a passivation layer on the semiconductor layer.

15. The method according to claim 12, wherein widths of the first and second dummy patterns are less than about 3/4 of a width of the sealant pattern.

16. The method according to claim 12, wherein each of the gate link portions comprise:

a gate metal layer on the first substrate;

a gate insulating layer on the gate metal layer;

a semiconductor layer on the gate insulating layer; and

a passivation layer on the semiconductor layer.

17. The method according to claim 12, wherein each of the data link portions comprise:

a gate insulating layer on the first substrate;

a semiconductor layer on the gate insulating layer;

a data metal layer on the gate insulating layer; and

a passivation layer on the data metal layer.

18. The method according to claim 12, wherein a height of the gate link portions and a height of the data link portions are substantially the same.